In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) An integrated circuit, comprising:

an array of memory cells, the array configured as a NAND array in a plurality of columns and rows of memory cells, the columns comprising one or more sets of memory cells in series coupled to a bit line, and the rows comprising sets of memory cells having their respective gate terminals coupled to a word line, memory cells in the array respectively comprising a gate terminal, a first channel terminal, a second channel terminal and a channel region between the first and second channel terminals, a charge trapping structure over the channel region, a tunneling dielectric between the channel region and the charge trapping structure, and a blocking dielectric between the charge trapping structure and the gate terminal;

circuitry to program the memory cells in the array by E-field assisted tunneling through the tunneling dielectric by applying a positive voltage to the gate terminal and a low voltage or ground to the first and second channel terminals, while limiting program and erase cycling; and

circuitry to read data from the memory cells.

2. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a barrier height and thickness sufficient to prevent direct tunneling.

3. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a silicon-dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.

4. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness greater than 30 Angstroms.

5. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness between about 30 Angstroms and about 70 Angstroms.

6. (original) The integrated circuit of claim 1, wherein the positive voltage is about 15 Volts or greater.

7. (original) The integrated circuit of claim 1, wherein the E-field is about 15 Volts over 5 nanometers, or higher.

8. (original) The integrated circuit of claim 1, wherein said array of memory cells is configured as a read only memory.

9. (original) The integrated circuit of claim 1, wherein memory cells in said array have a negative threshold voltage prior to programming.

10. (original) The integrated circuit of claim 1, wherein memory cells in said array of memory cells are configured for one-time programming.

11. (original) The integrated circuit of claim 1, including a static random access memory array, and logic which accesses data stored in said array of memory cells and the static random access memory array.

12. (original) The integrated circuit of claim 1, including a static random access memory array, and a processor which executes instructions, including instructions for access to data stored in said array of memory cells, and stored in the static random access memory array.

13. (original) The integrated circuit of claim 1, including a static random access memory array, and a processor which executes instructions, including instructions for access to data stored in said array of memory cells, and stored in the static random access memory array, and wherein said logic to program comprises instructions executed by the processor.

14. (original) The integrated circuit of claim 1, wherein the charge trapping structure comprises silicon nitride.

15. (currently amended) The integrated circuit of claim 1, wherein the charge trapping structure comprises ~~one or more of alumina, HfOx, ZrOx, or other~~ a metal oxide~~-material~~.

16. (original) A read only memory cell, comprising:

a first channel terminal;

a second channel terminal spaced away from the first channel terminal by a channel, and wherein the channel is configured to have a negative threshold prior to programming;

a charge trapping structure;

a gate;

a blocking dielectric between the charge trapping structure and the gate; and

a tunnel dielectric between the channel and the charge trapping layer, wherein the tunnel dielectric has a barrier height and thickness sufficient to prevent direct tunneling, the memory cell adapted for one-time programming by applying a positive voltage to the gate and a low voltage or ground to the first and second channel terminals, and adapted for use as a read only memory.

17. (currently amended) An integrated circuit on a single substrate, comprising:

an array of memory cells configured as read only memory, the array configured as a NAND array in a plurality of columns and rows of memory cells, the columns comprising one or more sets of memory cells in series coupled to a bit line, and the rows comprising sets of memory cells having their respective gate terminals coupled to a word line, memory cells in the array respectively comprising a gate terminal, a first channel terminal, a second channel terminal and a channel region between the first and second channel terminals, a charge trapping structure over the channel region, a tunneling dielectric between the channel region and the charge trapping structure, and a blocking dielectric between the charge trapping structure and the gate terminal

a plurality of word lines in the array contacting the gates of memory cells in respective rows in the array;

a plurality of bit lines in the array coupled to sets of memory cells along respective columns in the array;

an address decoder coupled to the plurality of word lines and the plurality of bit lines to address selected memory cells in the array;

logic, coupled to the plurality of word lines and the plurality of bit lines, to program the memory cells in the array E-field assisted tunneling of electrons to the charge trapping structure

by applying a positive voltage to the gate terminal and a low voltage or ground to the first and second channel terminals, while limiting program and erase cycling; and

sense circuitry, coupled to the plurality of bit lines, to sense threshold voltages in selected memory cells in the array.

18. (original) The integrated circuit of claim 17, wherein the tunneling dielectric has a silicon dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.

19. (original) The integrated circuit of claim 17, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness greater than 30 Angstroms.

20. (original) The integrated circuit of claim 17, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness between about 30 Angstroms and about 70 Angstroms.

21. (original) The integrated circuit of claim 17, wherein the positive voltage is about 15 Volts or greater.

22. (original) The integrated circuit of claim 17, wherein the E-field is about 15 Volts over 5 nanometers, or higher.

23. (original) The integrated circuit of claim 17, wherein memory cells in said array have a negative threshold voltage prior to programming.

24. (original) The integrated circuit of claim 17, wherein memory cells in said array of memory cells are configured for one-time programming.

25. (original) The integrated circuit of claim 17, including a static random access memory array, and logic which accesses data stored in said array of memory cells and the static random access memory array.

26. (original) The integrated circuit of claim 17, including a static random access memory array, and a processor which executes instructions, including instructions for access to data stored in said array of memory cells, and stored in the static random access memory array.

27. (original) The integrated circuit of claim 17, including a static random access memory array, and a processor which executes instructions, including instructions for access to data stored in said array of memory cells, and stored in the static random access memory array, and wherein said logic to program comprises instructions executed by the processor.

28. (original) The integrated circuit of claim 17, wherein the charge trapping structure comprises a layer of silicon nitride.

29. (currently amended) The integrated circuit of claim 17, wherein the charge trapping structure comprises a metal oxide ~~one or more of silicon nitride, HfO_2, etc~~.

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